ABSTRACT OF THE DISCLOSURE

A frequency and phase synchronizer system comprises a processor for executing a sequence of operations, which include: a) initializing a frequency error estimate value and phase error estimate value; b) separating discrete samples of a continuous phase modulation signal into a first sequence of odd numbered samples of the signal, and a second sequence of even numbered samples of the signal; c) determining an unknown frequency offset value from the first and second sequences, frequency error estimate, and phase error estimate; d) determining an unknown phase offset value from the first and second sequences, frequency error estimate, phase error estimate, and a first discrete data sample of said discrete samples of the continuous phase modulation signal; f) updating the frequency error estimate from the unknown frequency offset value; and updating the phase error estimate from the unknown phase offset value.